Amendment to the Claims:

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This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently amended) A method comprising:

receiving a request for access to a memory location;

identifying a memory block including the memory location;

examining a local memory descriptor associated with said memory block; and

accessing a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory, wherein the local addressable memory is at the same level of memory as a separate local cache.

2. (Original) The method of claim 1, further comprising accessing the memory location in response to the memory location existing in the local addressable memory.

3. (Original) The method of claim 1, further comprising generating an illegal access violation exception in response to the memory location not existing in the local addressable memory.

4. (Original) The method of claim 1, further comprising accessing a local cache in response to the local memory descriptor indicating that the memory block is not in the local addressable memory.

5. (Original) The method of claim 1, wherein said receiving a request for access to a memory location comprises receiving an address.

6. (Original) The method of claim 5, wherein said identifying a memory block including the memory location comprises identifying a page having an address space including said address.

7. (Original) The method of claim 1, wherein accessing a local addressable memory comprises accessing a Level 1 (L1) SRAM (Static Random Access Memory).

8. (Original) The method of claim 7, wherein said examining a local memory descriptor comprises examining the state of an L1 SRAM bit associated with the memory block.

9. (Original) The method of claim 7, wherein said examining a local memory descriptor comprises examining a cacheability Protection Look-aside Buffer (CPLB) descriptor including an L1 SRAM bit associated with the memory block.

10. (Original) The method of claim 7, wherein said examining a local memory descriptor comprises examining a Translation Look-aside Buffer (TLB) descriptor including an L1 SRAM bit associated with the memory block.

11. (Currently amended) A method comprising:
receiving a request for access to a memory location;

identifying a memory block including the memory location; and

routing the request to one of a local addressable memory and a local cache in response to the state of a local memory descriptor associated with said memory block, wherein the local addressable memory is at the same level of memory as a separate local cache.

12. (Original) The method of claim 11, further comprising accessing the local addressable memory.

13. (Original) The method of claim 11, further comprising generating an illegal access violation exception in response to the memory location not existing in the local addressable memory.

14. (Original) The method of claim 11, wherein accessing a local addressable memory comprises accessing a Level 1 (L1) SRAM (Static Random Access Memory).

15. (Currently amended) An apparatus comprising:

an execution unit;

a local addressable memory;

a separate local cache at the same level of memory as the local addressable memory; and

a local memory controller operative to identify a memory block including a memory location in response to receiving a request for access to said memory location from the execution unit and to route the request to one of the local addressable memory and the local cache in response to the state of a local memory descriptor associated with said memory block.

16. (Original) The apparatus of claim 15, further comprising a plurality of local memory descriptors associated with a plurality of memory blocks.

17. (Original) The apparatus of claim 15, wherein the local addressable memory comprises a Level 1 (L1) SRAM (Static Random Access Memory).

18. (Original) The apparatus of claim 17, wherein the local memory descriptor comprises an L1 SRAM bit indicating whether an associated memory block resides in the local memory.

19. (Currently amended) A system comprising:

a processor including

an execution unit,

a local addressable memory,

a separate local cache at the same level of memory as the local addressable memory, and

a local memory controller operative to identify a memory block including a memory location in response to receiving a request for access to said memory location from the execution unit and to route the request to one of the local addressable memory and the local cache in response to the state of a local memory descriptor associated with said memory block; and

a USB (Universal Serial Bus) interface; and

a system bus coupled to the processor and the USB interface.

20. (Original) The system of claim 19, wherein the local addressable memory comprises a Level 1 (L1) SRAM (Static Random Access Memory).

21. (Currently amended) An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

receive a request for access to a memory location;

identify a memory block including the memory location;

examine a local memory descriptor associated with said memory block; and

access a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory, wherein the local addressable memory is at the same level of memory as a separate local cache.

22. (Original) The article of claim 21, further comprising instructions operative to cause the machine to access the memory location in response to the memory location existing in the local addressable memory.

23. (Original) The article of claim 21, further comprising instructions operative to cause the machine to generate an illegal access violation exception in response to the memory location not existing in the local addressable memory.

24. (Original) The article of claim 21, further comprising instructions operative to cause the machine to access a local cache in response to the local memory descriptor indicating that the memory block is not in the local addressable memory.

25. (Currently amended) An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

receive a request for access to a memory location;

identify a memory block including the memory location; and

route the request to one of a local addressable memory and a local cache in response to the state of a local memory descriptor associated with said memory block, wherein the local addressable memory is at the same level of memory as a separate local cache.

26. (Original) The article of claim 25, further comprising instructions operative to cause the machine to:

access the local addressable memory; and

generate an illegal access violation exception in response to the memory location not existing in the local addressable memory.

27. (Original) The method of claim 25, wherein the instructions operative to cause the machine to access a local addressable memory include instructions operative to cause the machine to access a Level 1 (L1) SRAM (Static Random Access Memory).

28. (Currently amended) A method comprising:

accessing a local memory configurable as one of a Static Random Access Memory (SRAM) and a cache, wherein the local memory is at the same level of memory as a separate local cache;

configuring the local memory as SRAM; and

extending a local memory address space to the local memory.

29. (Previously Presented) The method of claim 28, wherein said extending the local memory space comprises setting a bit in a memory descriptor.

30. (Currently amended) An article comprising:

a machine-readable medium which stores machine-executable instructions, the instructions operative to cause a machine to:

access a local memory configurable as one of a Static Random Access Memory (SRAM) and a cache, wherein the local memory is at the same level of memory as a separate local cache;

configure the local memory as SRAM; and

extend a local memory address space to the local memory.

31. (Previously Presented) The article of claim 30, wherein the instructions operative to cause the machine to extend the local memory space include instructions operative to cause the machine to set a bit in a memory descriptor.

32. (Currently amended) A method comprising:

receiving a request for access to a memory location;

identifying a memory block including the memory location;

examining a local memory descriptor associated with said memory block;

accessing a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory; and

accessing a separate local cache in response to the local memory descriptor indicating that the memory block is not in the local addressable memory, wherein the local addressable memory is at the same level of memory as the local cache.

33. (new) The method of claim 7, wherein the local cache comprises an L1 cache.

34. (new) The method of claim 14, wherein the local cache comprises an L1 cache.

35. (new) The apparatus of claim 17, wherein the local cache comprises an L1 cache.

36. (new) The system of claim 20, wherein the local cache comprises an L1 cache.

37. (new) The method of claim 27, wherein the local cache comprises an L1 cache.

38. (new) The method of claim 28, wherein the local memory comprises a Level 1 (L1) memory.

39. (new) The article of claim 30, wherein the local memory comprises a Level 1 (L1) memory.

40. (new) The method of claim 32, wherein the same level of memory is Level 1 (L1) memory.